ABSTRACT

A pipeline accelerator includes a memory and a hardwired-pipeline circuit coupled to the memory. The hardwired-pipeline circuit is operable to receive data, load the data into the memory, retrieve the data from the memory, process the retrieved data, and provide the processed data to an external source. In addition or in the alternative, the hardwired-pipeline circuit is operable to receive data, process the received data, load the processed data into the memory, retrieve the processed data from the memory, and provide the retrieved processed data to an external source. Where the pipeline accelerator is coupled to a processor as part of a peer-vector machine, the memory facilitates the transfer of data — whether unidirectional or bidirectional — between the hardwired-pipeline circuit(s) and an application that the processor executes.